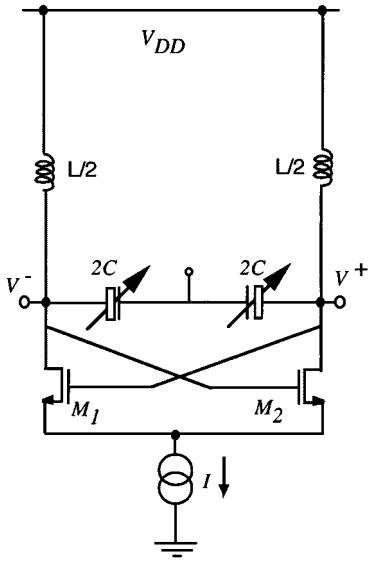

Fig. 9. Diagram of the LC CMOS VCO employing one cross-coupled pair.

based on the topology of Fig. 9, shows the highest FOM. Nonetheless, we still support the topology proposed here for the following reasons

- To achieve such a high FOM, the oscillation amplitude of the topology of Fig. 9 is well above the supply voltage (in principle, it can be twice as much). This means that the supply voltage has to be kept lower than the maximum value allowed by the technology and the oscillation amplitude must be limited to guarantee process reliability.
- The noise contribution of the tail current source transistor is intrinsically smaller in this topology (one-half everything else being the same) since the same oscillation amplitude is achieved with one-half the biasing current.

In addition, the MOS varactor Q will benefit from scaling. As a consequence, the quality factor of a tank using bond-wire inductors and the proposed MOS varactor will improve in further scaled technologies since the varactor limits the achievable Q.

V. Conclusions

This paper has provided the guidelines for the optimization of a CMOS LC VCO in terms of phase noise times power consumption, i.e., the actual parameter of interest. Equation (6) represents its theoretical minimum. Optimized CMOS VCOs compare favorably with their bipolar counterparts. To achieve very low FOM in future scaled technologies, tanks realized by means of bond-wire inductors are very attractive.

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Interface Loss Mechanism of Millimeter-Wave Coplanar Waveguides on Silicon

W. Zhao, C. Schöllhorn, and E. Kasper

***Abstract*—The interface loss mechanisms of coplanar waveguides (CPWs) on silicon with an SiO_2 isolation layer are investigated. The total losses of straight CPW lines of 7.5-mm length are measured between 45 MHz and 40 GHz and the interface contribution is extracted from that by its bias dependence. The interface losses depend on bias voltage and on the oxide quality. With an optimal bias voltage, the attenuation of a CPW with an unpatterned oxide layer always achieves a minimum. With bias between the flat-band voltage V_{FB} and threshold voltage V_{T} (depletion region), the interface losses are negligible. For high quality oxides (V_{T} around 0 V), very low attenuation was obtained without any bias.**

***Index Terms*—Bias-dependent attenuation, coplanar waveguide, depletion, interface losses, oxide, silicon, threshold voltage.**

I. Introduction

Low-doped silicon ($<10^{13}$ charge carriers per cm^3) is a suitable semiconductor substrate for low-loss microwave applications [1], [2]. The low-doped silicon is usually manufactured by a highly pure float

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The authors are with the Institut für Halbleitertechnik, Universität Stuttgart, D-70569 Stuttgart, Germany (e-mail: zhao@iht.uni-stuttgart.de).

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zone (FZ) process with a resistivity over 1000 $\Omega \cdot$ cm. Microwave circuits on high-resistivity silicon are known as silicon monolithic microwave integrated circuits (SIMMWICs) [3]. In semiconductor microwaves circuits [(i.e., monolithic microwave integrated circuits (MMIC)] preferably gold (Au) is used as standard metallization. In this technology, the thin start layer is increased to a thickness of a few micrometers with a galvanic process. Gold is soft and stainless, which makes the "on wafer" measurement and the connection technique (bonding, flip chip) easier. Most SIMMWIC circuits are designed with a microstrip transmission line, which causes additional technological efforts for substrate thinning and for etching via holes to realize connection to the ground on the backside metallization. In contrast, coplanar waveguides (CPWs) are much easier to integrate into circuits because signal and ground metallization are lying in a single plane. In the dominant silicon microelectronics manufacturing aluminum (Al) with a thickness of 1 μm is used as a standard metal. For high complex and strongly miniaturized circuits ($\leq$0.18-μm CMOS), copper (Cu) is increasingly used as material for the metal interconnects.

Device miniaturization and the use of heterostructures (SiGe/Si) shift the limitation for the use of silicon-based transistors into the microwave and millimeter-wave regions so that, in the future, the range of applications can be substantially increased by SIMMWIC circuits. At the same time, it gets more and more important to use the standard metallization of silicon microelectronics (i.e., aluminum) for the SIMMWIC circuits.

An isolation layer, e.g., oxide or nitride, in the integrated circuits between the waveguides and substrate is necessary in order to avoid leakage currents and possible shorts. Higher attenuation occurs unexpectedly in the CPWs with the isolation layer. In [4], the effects of the SiO_2 layer between the metal and high-resistivity silicon were reported and as solution suggested, for example, an implanted layer as "channel stop." Gamble *et al.* [5] used poly-Si between SiO_2 and monocrystalline silicon to reduce the high total attenuation.

In this paper, we investigated the interface loss mechanisms of CPWs on high-resistivity silicon substrates with an SiO_2 isolation layer and its bias dependence. Experimental investigations were performed with 1-μm aluminum interconnects. The conditions are determined under which low-loss operation of CPW circuits may be obtained.

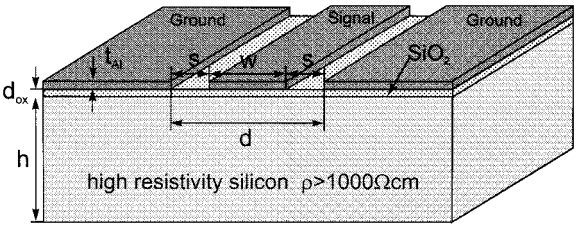


Fig. 1. Sketch of the important lateral and vertical dimensions of a CPW.

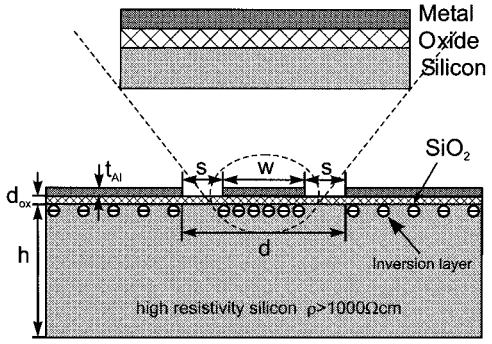


Fig. 2. CPW on high-resistivity silicon as a MOS varactor with an inversion layer at the interface.

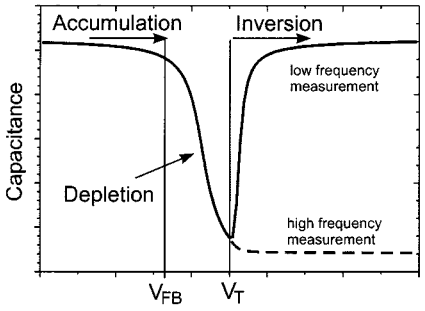


Fig. 3. CV characteristics of a MOS varactor.

II. Interface Loss Mechanism of CPWs

There are many descriptions of the conductor losses and the dielectric substrate losses in the literature [6]–[12]. We additionally investigate the contribution of the interface losses. Fig. 1 shows a CPW. The metal layer (signal line and ground plane) with a typical thickness of $t_{\rm Al} = 1$ μm is deposited on an insulating oxide layer top of the substrate. As a substrate, we used high-resistivity silicon with resistivity $\rho > 1000\ \Omega \cdot$ cm.

The structure of a coplanar transmission line can be regarded as an MOS varactor (metal–oxide semiconductor) [13] (Fig. 2). With a bias voltage, the MOS varactor can be switched from accumulation over depletion into inversion and vice versa. This effect can be proven by a capacitance voltage (CV) measurement. A typical CV curve is shown in Fig. 3. The ideal operating condition of the coplanar transmission line is in the depletion region. In this case, there are no induced charge carriers at the interface. The number of free charge carriers at the interface can vary within a wide range. It depends on the bias voltage. For high-resistivity silicon (10^{13} cm^{-3} p-type, approximately 1000 $\Omega \cdot$cm) with metal on a 200-nm-thick oxide, the interface carrier concentration can reach $p = 5 \cdot 10^{17}$ cm^{-3} in accumulation for a bias voltage of -5 V or $n = 8.5 \cdot 10^{17}$ cm^{-3} in the inversion case for a voltage of $+5$ V. These induced charge carriers between the oxide and silicon substrate lead to additional losses, which we call interface losses. This part of the losses depends on the bias voltage. With a proper bias voltage that shifts the interface into the depletion state, it is possible to reach a minimum in the total losses of the CPW.

The onset of the inversion state is given by the threshold voltage ($V_{\rm T}$)

$$V_{\rm T} = V_{\rm FB} - \frac{Q_S + Q_i}{c_{\rm ox}} + 2\psi_S$$

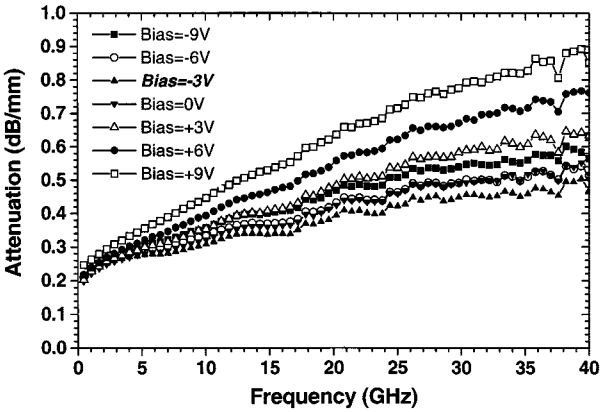
with flat-band voltage $V_{\rm FB}$, surface potential ψ_S, bulk charges Q_S, area-specific oxide capacitance $c_{\rm ox}$, and interface state density Q_i.

The threshold voltage $V_{\rm T}$ is shifted by the positive interface state density Q_i into the negative direction. The charges in the oxide influence the flat-band voltage $V_{\rm FB}$ and, thus, also the threshold voltage $V_{\rm T}$. Therefore, the oxide quality plays a very important role. It should be clearly stated that not the interface charge itself, but the free carriers (either in accumulation or inversion) influenced by the charge are responsible for the interface losses. For a high-resistivity silicon (small Q_S) and a relatively thick insulating oxide (small $c_{\rm ox}$), the interface state density Q_i has an even stronger influence on the threshold voltage $V_{\rm T}$ than in a usual MOS transistor configuration. Table I shows the calculated threshold voltage $V_{\rm T}$ with a different interface state density Q_i.

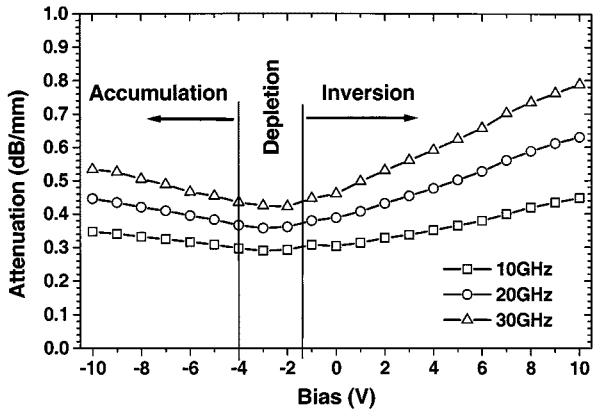
If a threshold voltage is shifted by a bad oxide quality onto $V_{\rm T} = -5$ V, the CPW is operated with zero bias in the inversion state. In this case, a surface charge density in silicon immediately under oxide

TABLE I
RELATIONSHIP BETWEEN OXIDE QUALITY (INTERFACE STATE DENSITY Q_i) AND THRESHOLD VOLTAGE V_T FOR HIGH-RESISTIVITY SILICON WITH $N_A = 10^{13}/\text{cm}^3$ AND AN OXIDE THICKNESS $d_{ox} = 200$ nm ($\Phi_{Al} = 4.08$ eV, $\chi_{Si} = 4.05$ eV, $E_g = 1.12$ eV AND $q = 1.6 \cdot 10^{-19}$ As)

Oxide quality	Interface state density Q_i	threshold voltage V_T
excellent	0 q/cm^2	-0.28V
very good	10^{10} q/cm^2	-0.37V
good	10^{11} q/cm^2	-1.21V
bad	10^{12} q/cm^2	-9.55V
very bad	10^{13} q/cm^2	-92.95V



(a)



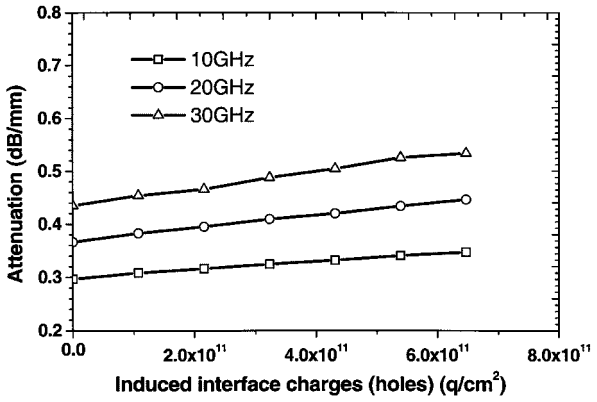
(b)

Fig. 4. (a) Attenuation versus frequency of aluminum CPWs with different bias voltages ($w = 20\ \mu$m, $d = 50\ \mu$m, $t_{Al} = 1\ \mu$m, $\rho_{Si} > 1000\ \Omega \cdot$ cm, FZ Si). (b) Attenuation versus bias voltage for 10, 20, and 30 GHz.

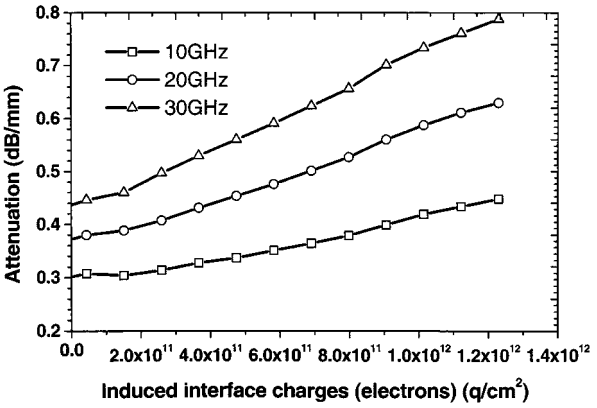
is induced $Q = c_{ox}(-V_T) = 5.4 \cdot 10^{11}$ q/cm^2. These charges in silicon contribute to the total losses. The contribution of these interface losses is normally larger than the contribution of the substrate losses in a high-resistivity silicon. Due to this, the quality of the oxide is the main factor for optimum "zero-bias" operation of a coplanar transmission line.

III. EXPERIMENTAL RESULTS

We used high-resistivity silicon (FZ Si) with $\rho_{Si} > 1000\ \Omega \cdot$ cm as substrate. First, a thin rapid thermal processing (RTP) oxide with good



(a)



(b)

Fig. 5. Relationship between the losses and induced interface charges. Same waveguide geometry as in Fig. 4. (a) Accumulation region. Induced interface charge is $(c_{ox} \cdot (V_{FB} - V))$. (b) Inversion region. Induced interface charge is $(c_{ox} \cdot (V - V_T))$.

TABLE II
ATTENUATION (IN DECIBELS PER MILLIMETERS) OF ALUMINUM (1 μm) CPWS ($w = 20\ \mu$m AND 45 μm) ON FZ SILICON ($\rho_{Si} > 1000\ \Omega \cdot$ cm) WITH OPTIMUM BIAS VOLTAGE

Frequency f		10GHz	20GHz	30GHz	40GHz
Attenuation (dB/mm)	w =20μm, d =50μm	0.30	0.39	0.45	0.48
	w =45μm, d =95μm	0.19	0.24	0.29	0.33

quality was grown at a temperature of 1150 °C. The thickness of this oxide is 200 nm and it is not patterned. A very good oxide quality is necessary in order to receive a threshold voltage close to 0 V for the "zero-bias" operation. Second, a 1-μm-thick aluminum metallization was sputtered and then patterned.

The attenuation of processed aluminum coplanar transmission lines in different dimensions and lengths was measured by carefully calibrated S-parameter measurements under a defined bias voltage. The bias dependency of interface carriers was additionally controlled by CV measurement.

Fig. 4(a) shows the measured curves with different bias voltages. The attenuation of this coplanar transmission line ($w = 20\ \mu$m, $d = 50\ \mu$m, $t_{Al} = 1\ \mu$m, $d_{ox} = 0.2\ \mu$m, $l = 7.5$ mm, $\rho_{Si} > 1000\ \Omega \cdot$ cm) achieved a minimum for a bias voltage $V = -3$ V. By applying a positive or strongly negative bias voltage, the transmission line is turned into inversion (positive voltage) and into accumulation (negative voltage), respectively. In both cases, the attenuation rises. The curves

of the bias-dependent attenuation at 10, 20, and 30 GHz are shown in Fig. 4(b). For a bias voltage between -4 and -1.5 V, the MOS structure is in the depletion region. This leads to a minimum in attenuation.

In the inversion region ($V > V_{\mathrm{T}}$) and accumulation region ($V < V_{\mathrm{FB}}$), the losses increase proportionally with increasing bias voltage $|V_{\mathrm{FB}} - V|$ or $|V - V_T|$. Fig. 5(a) and (b) shows the relationship between the losses and induced interface charges ($c_{\mathrm{ox}} \cdot (V_{\mathrm{FB}} - V)$ in the accumulation region and $c_{\mathrm{ox}} \cdot (V - V_T)$ in the inversion region). These induced interface charges are responsible for the strong scattering of the values of the total losses in the literature because V_{T} varies among different oxides. Thus, we separate this part as interface losses from the total losses. In the inversion region ($V > V_{\mathrm{T}}$), the losses are higher than in the accumulation region ($V < V_{\mathrm{FB}}$) because the mobility of the electrons is three times higher than those of the holes.

Table II shows the attenuation for different signal linewidths w. All measurements were performed at aluminum coplanar transmission lines on FZ silicon with a aluminum thickness of 1 μm. As expected, the attenuation increases with increasing frequency and decreases with increasing signal linewidth w.

IV. Conclusion

The three loss mechanisms of coplanar transmission lines, conductor losses in the metallization, substrate losses caused by the finite conductivity of the semiconductor, and interface losses caused by induced charges at the interface between insulator and semiconductor are responsible for the main part of the observed losses. The influence of the interface losses have been recognized and a way to decrease the total losses that have been described. The interface losses depend very much on the oxide quality (interface state density). They are responsible for the strong scattering of the values indicated in the literature for the total losses. The interface losses depend on the bias voltage. Between the flat-band voltage V_{FB} and the threshold voltage V_{T} (depletion region), the interface losses are negligible. In the inversion region, the losses are higher than in the accumulation region because the mobility of the electrons is three times higher than those of the holes. For the design of SIMMWIC circuits, it is important to separate the dc supply lines from the RF signal lines so that, on CPWs, zero bias voltage is applied, which should bring the CPW with an oxide layer into a depletion state.

The attenuation of the aluminum CPW, when combined with an oxide layer of good quality, shows acceptable values with an optimal bias voltage close to 0 V. The aluminum metallization of standard silicon microelectronics technology is suitable for millimeter-wave applications when oxides with good interface quality are used. A quantitative description of the effect needs further investigation.

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